

**IN THE CLAIMS:**

21. – 23 (Cancelled)

24. (Currently Amended) A method of fabricating an EEPROM semiconductor device having a plurality of memory cell transistors, comprising :

forming a plurality of field insulating films in parallel with one another in a first direction on a semiconductor substrate, each of said plurality of field insulating films provided for a plurality of memory cell ~~transistors~~ transistors, and said plurality ~~a plurality~~ of memory cell transistors formed between two associated adjacent field insulating films;

forming a first gate insulating film in each of active regions;

forming a plurality of first polysilicon films ;

patterning said first polysilicon film to form first polysilicon strips in parallel with one another, said first polysilicon strips formed in said first direction;

forming a second gate insulating film on said first polysilicon strips

forming a second ~~polysilicon~~ polysilicon layer on said second gate insulating film;

patterning said second polysilicon layer, said second gate insulating film, said plurality of first polysilicon strips and said first gate insulating film to form a plurality of control gates, a plurality of second gate insulators, a plurality of floating gates, and a plurality of first gate insulators, respectively;

forming drain and source regions;

forming a first interlayer insulating layer on an entire surface of said semiconductor substrate;

forming contact-holes through said first interlayer insulating layer in alignment with said drain and source regions; and

forming a first metal wiring layer on said first interlayer insulating layer and filing said contact-holes therewith to couple said first wiring layer to a corresponding one of said drain and source regions in a memory area and a wiring layer of a logic area;

forming a second metal wiring layer which is patterned so as to form a common source line connecting said source regions with each other; and

forming aluminum backing wiring layers connecting to said plurality of control gates, simultaneously with forming said common source line.

25. (Cancelled)

26. (Previously Amended) The method as set forth in claim 24, wherein said backing wiring layers are constituted of said second metal wiring layer.

27.(New) The method as set forth in claim 24, wherein said second gate insulating film has a three-layered structure of oxide/nitride/oxide films.

28.(New) The method as set forth in claim 24, wherein said first and second metal wiring layers are composed of aluminum.